FIG. 1

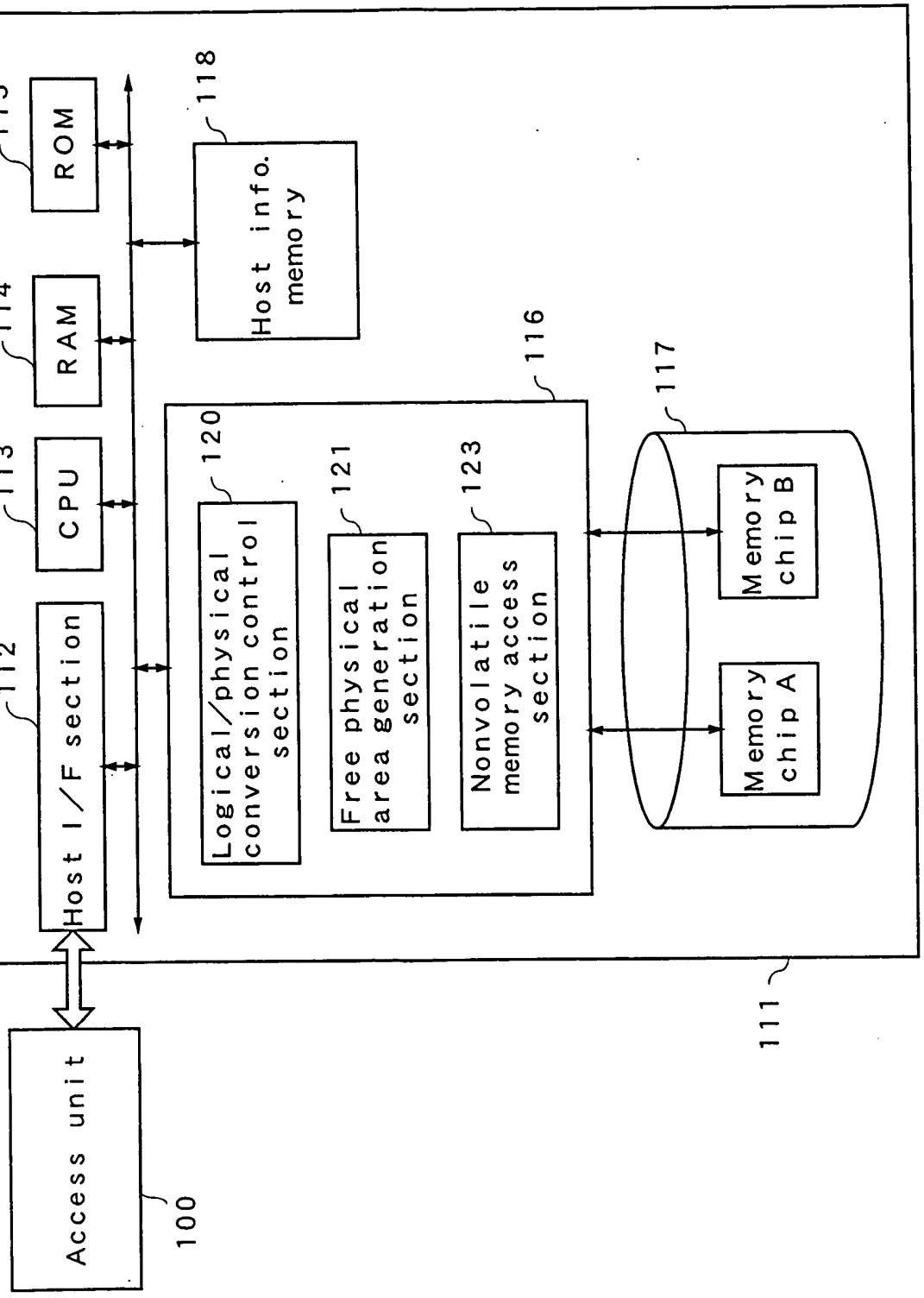
Access unit
100
Host I/F section
112
CPU
113
RAM
114
ROM
115
Host info. memory
118
Logical/physical conversion control section
120
Free physical area generation section
121
Nonvolatile memory access section
123
116
117
Memory chip A
Memory chip B
111

FIG. 2

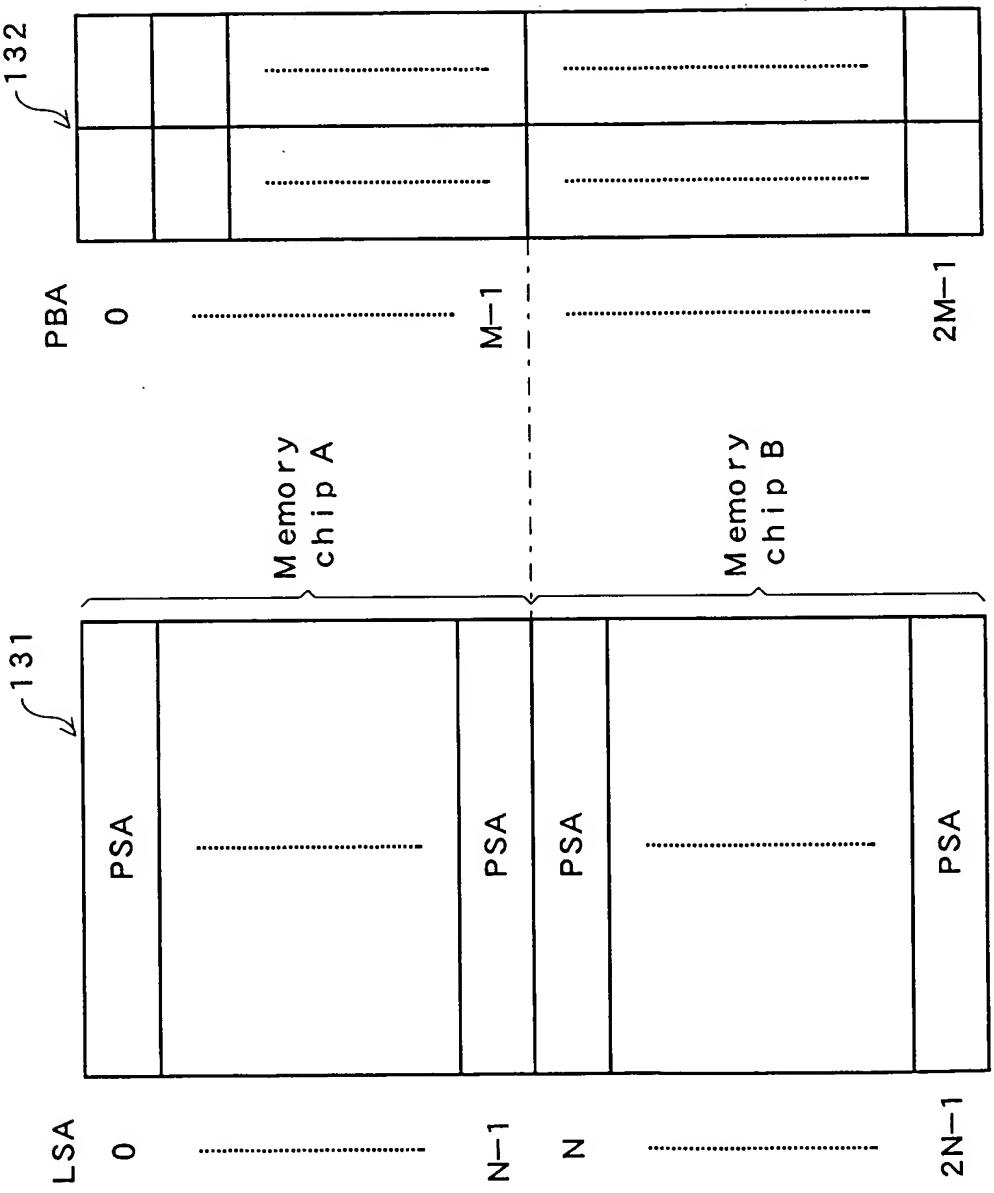
132
PBA
0
M−1
2M−1
Memory chip A
Memory chip B
131
PSA
PSA
PSA
PSA
LSA
0
N−1
N
2N−1

FIG. 3

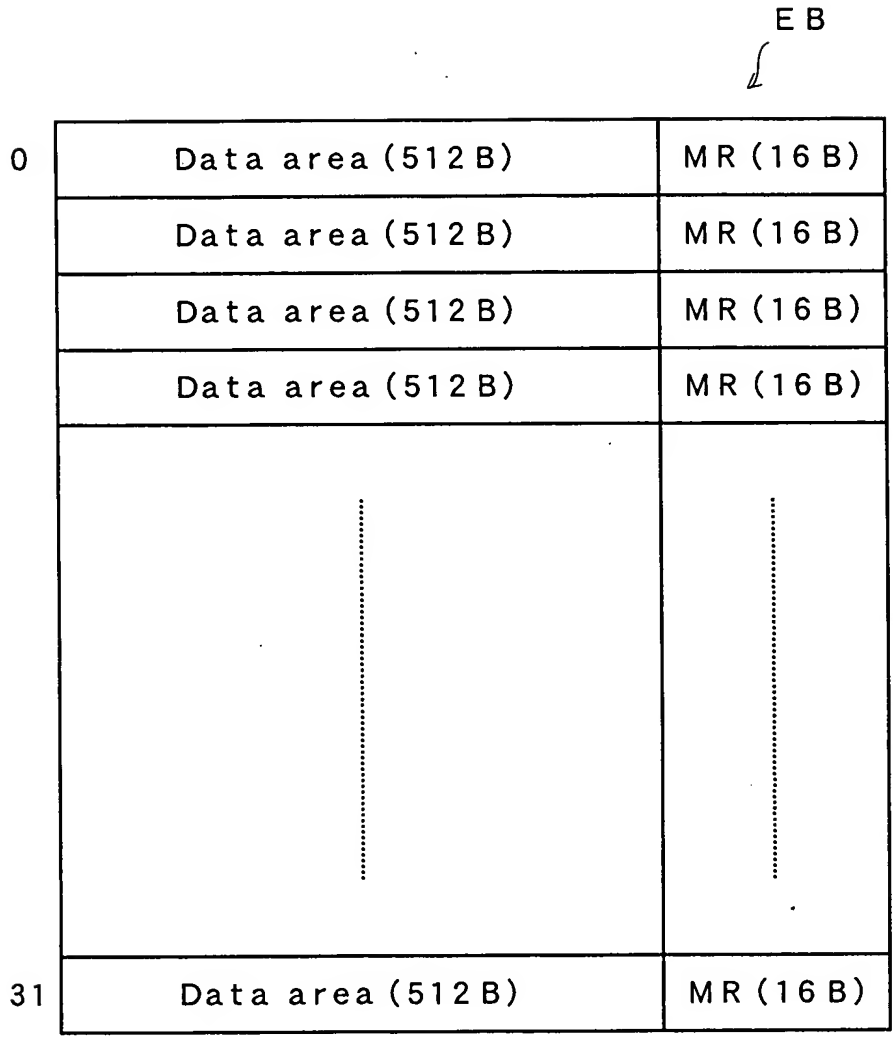
EB
0
Data area (512B)
MR (16B)
Data area (512B)
MR (16B)
Data area (512B)
MR (16B)
Data area (512B)
MR (16B)
31
Data area (512B)
MR (16B)

FIG. 4

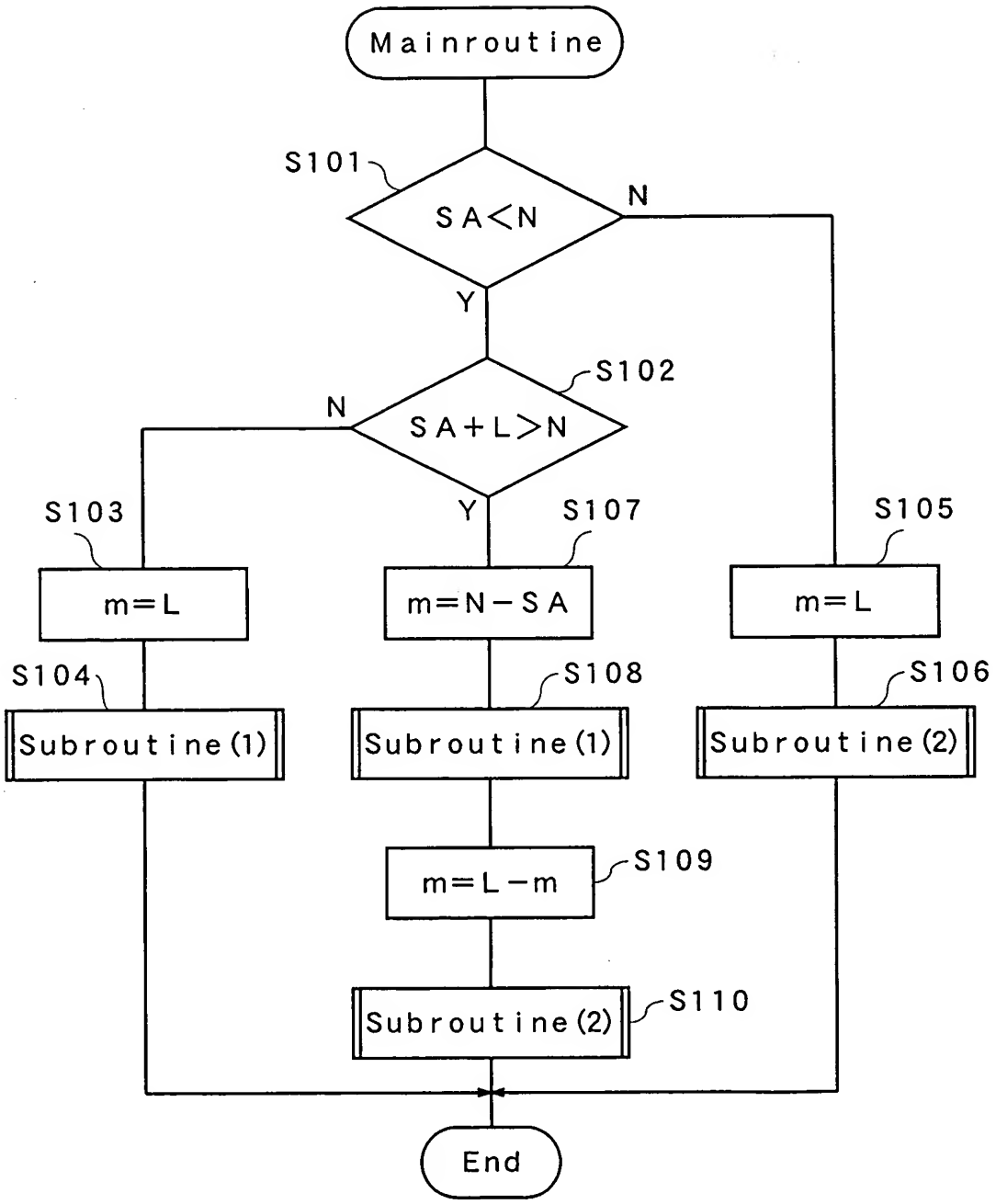
Mainroutine
S101
SA<N
N
Y
S102
N
SA+L>N
Y
S103
S107
S105
m=L
m=N−SA
m=L
S104
S108
S106
Subroutine(1)
Subroutine(1)
Subroutine(2)
m=L−m
S109
Subroutine(2)
S110
End

FIG. 5

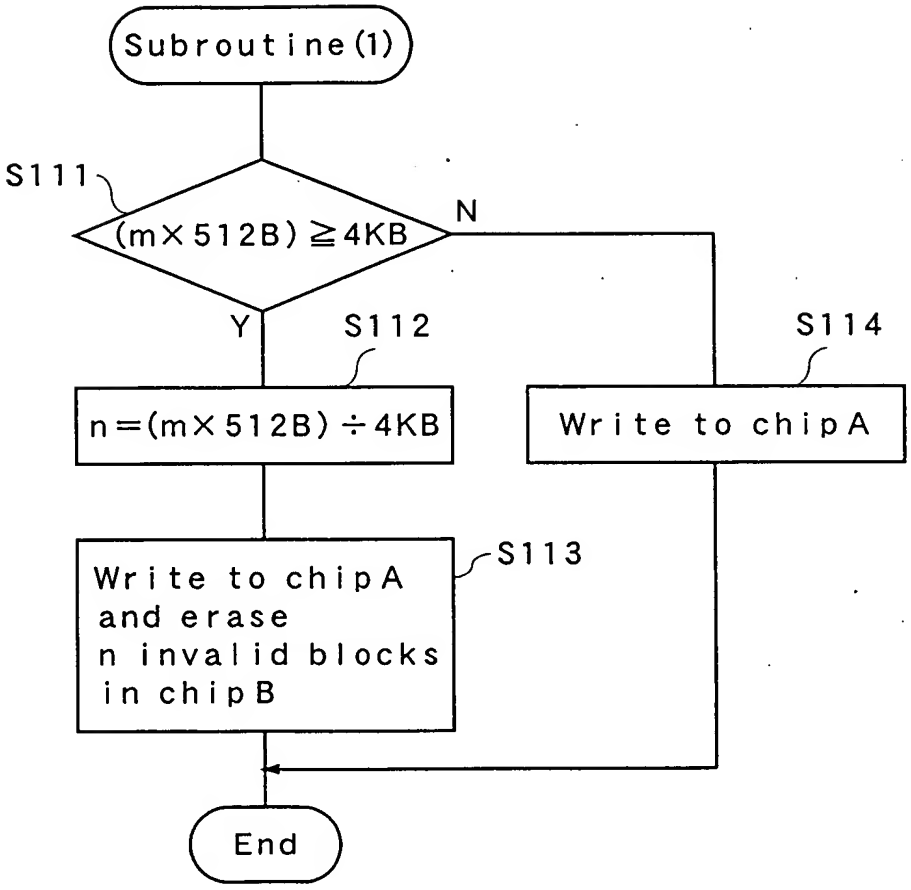
Subroutine(1)
S111
(m×512B)≧4KB
N
Y
S112
S114
n=(m×512B)÷4KB
Write to chipA
S113
Write to chipA
and erase
n invalid blocks
in chipB
End

FIG. 6

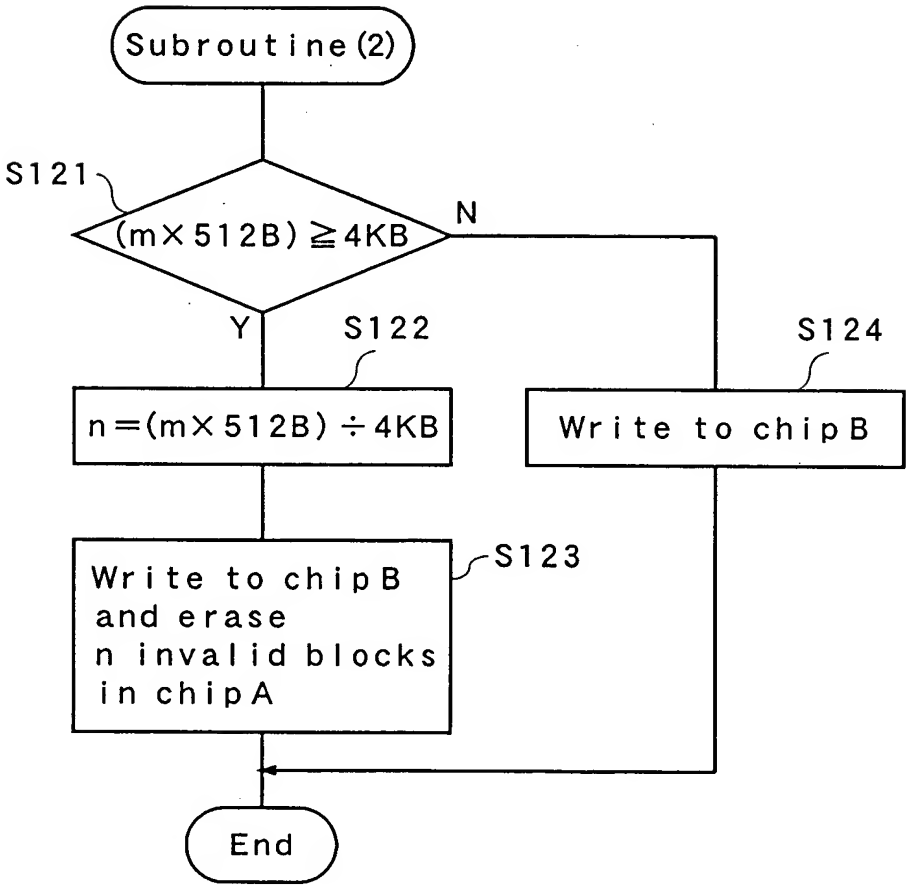
Subroutine(2)
S121
(m×512B)≧4KB
N
Y
S122
n=(m×512B)÷4KB
S124
Write to chipB
Write to chipB and erase n invalid blocks in chipA
S123
End

FIG. 7

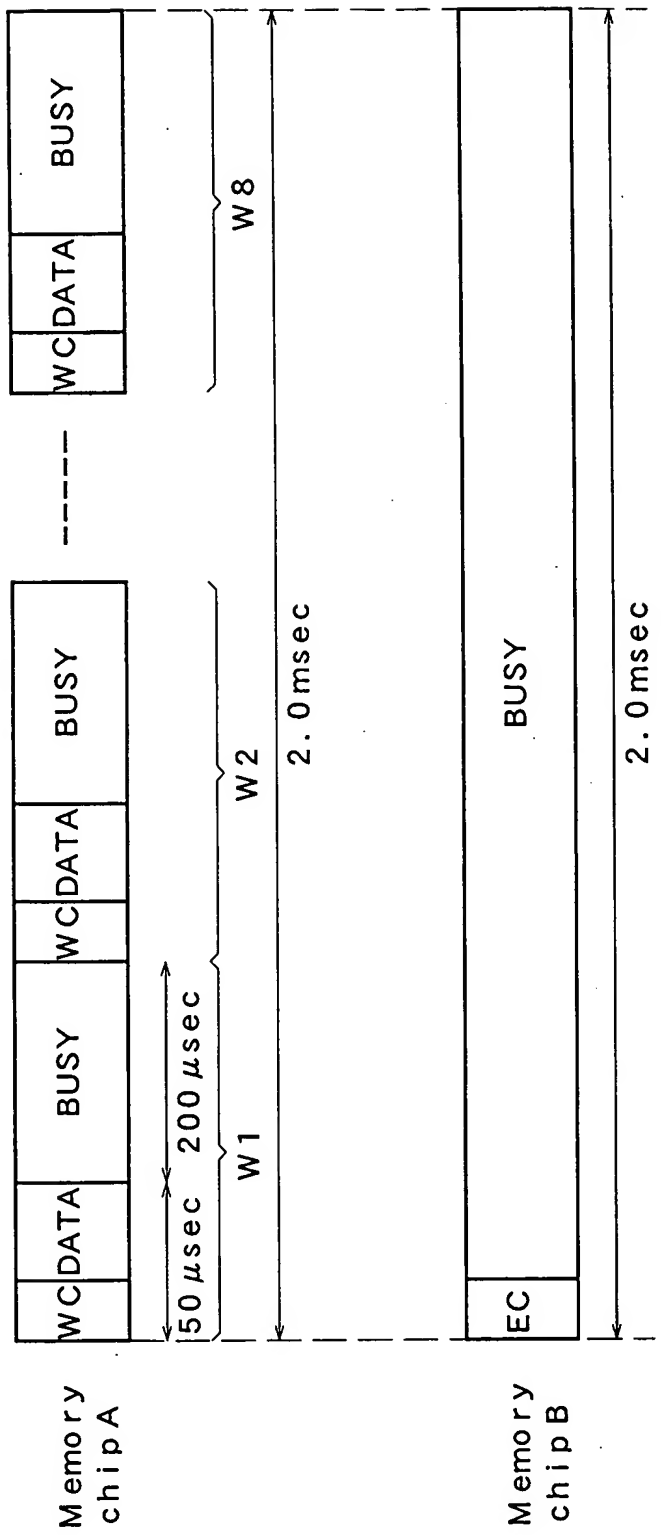
Memory chipA
WC
DATA
BUSY
WC
DATA
BUSY
50 μsec
200 μsec
W1
W2
2.0msec
WC
DATA
BUSY
W8
Memory chipB
EC
BUSY
2.0msec

FIG. 8

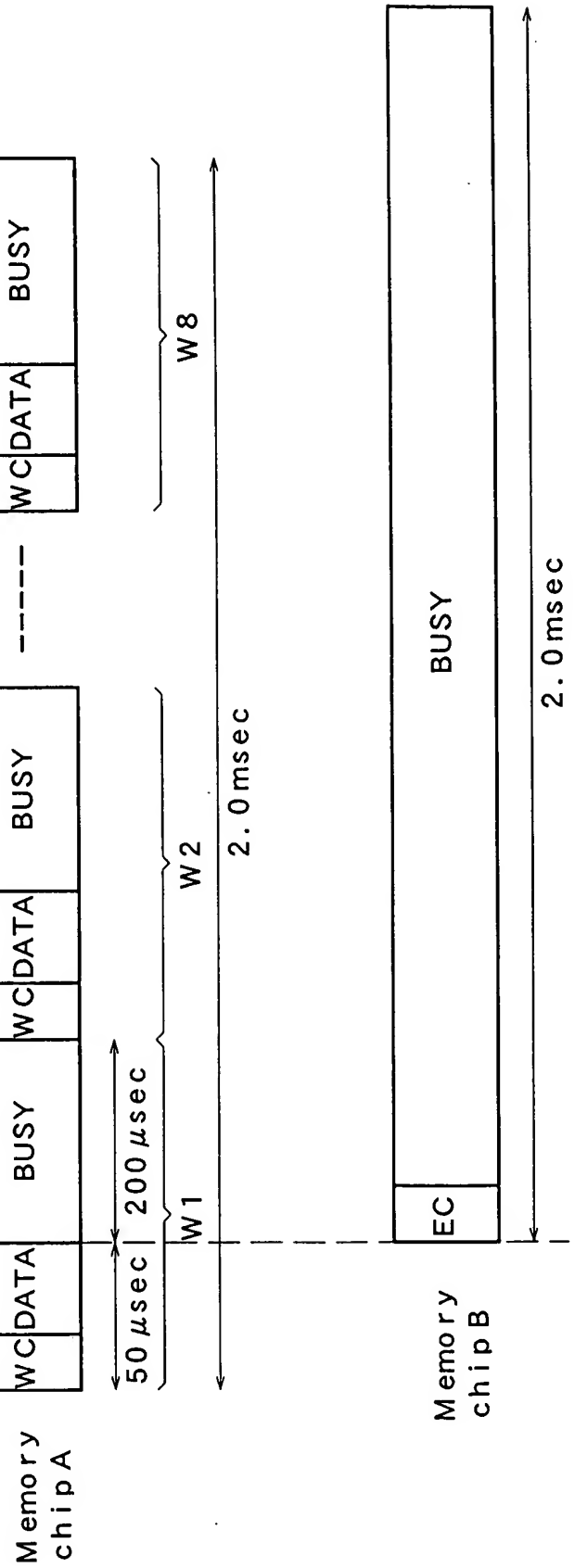
Memory chip A
WC
DATA
BUSY
WC
DATA
BUSY
50 μsec
200 μsec
W1
W2
2.0msec
WC
DATA
BUSY
W8
Memory chip B
EC
BUSY
2.0msec

FIG. 9

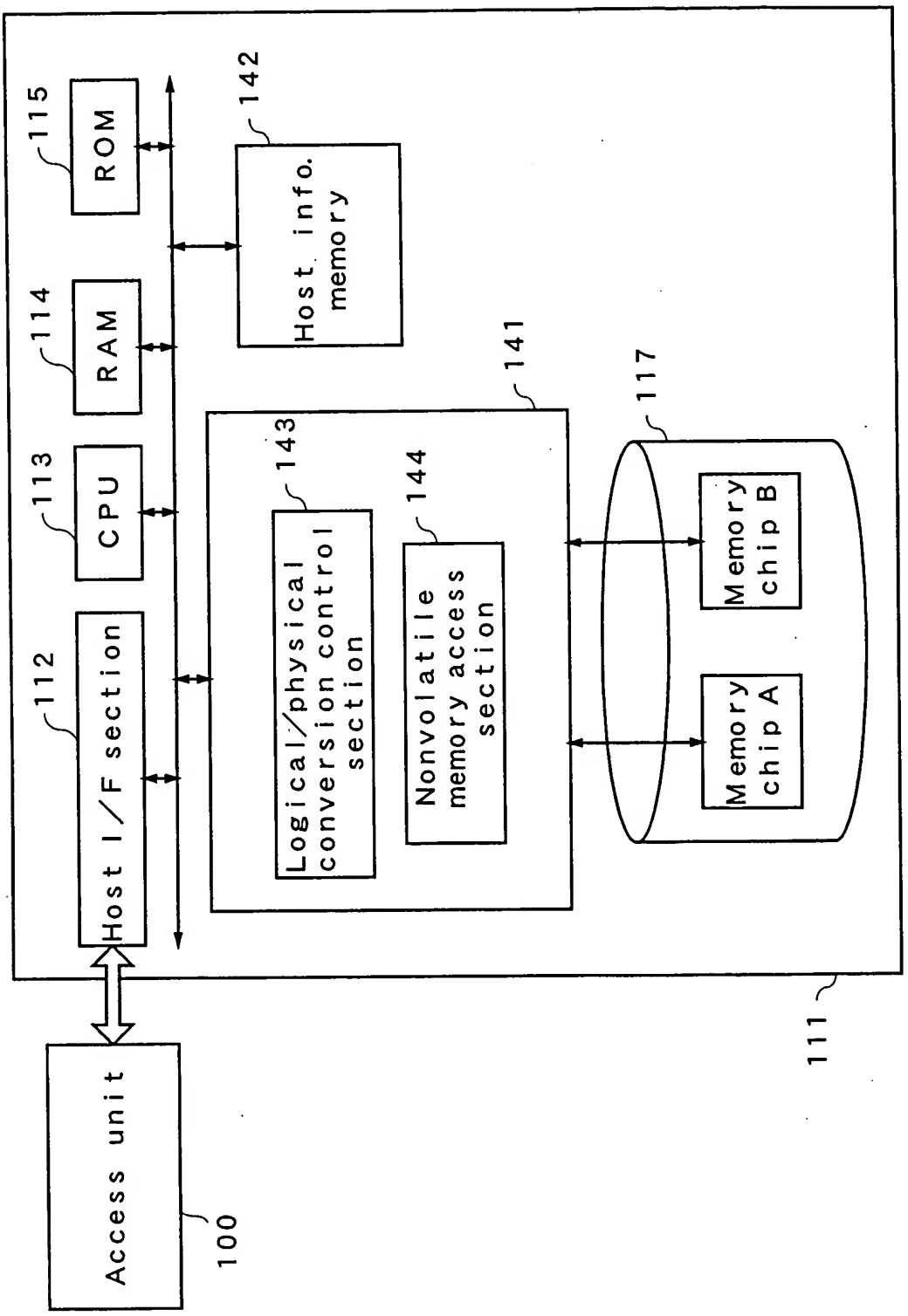
Access unit
100
111
Host I/F section
112
CPU
113
RAM
114
ROM
115
Host info. memory
142
141
Logical/physical conversion control section
143
Nonvolatile memory access section
144
117
Memory chip A
Memory chip B

FIG. 10

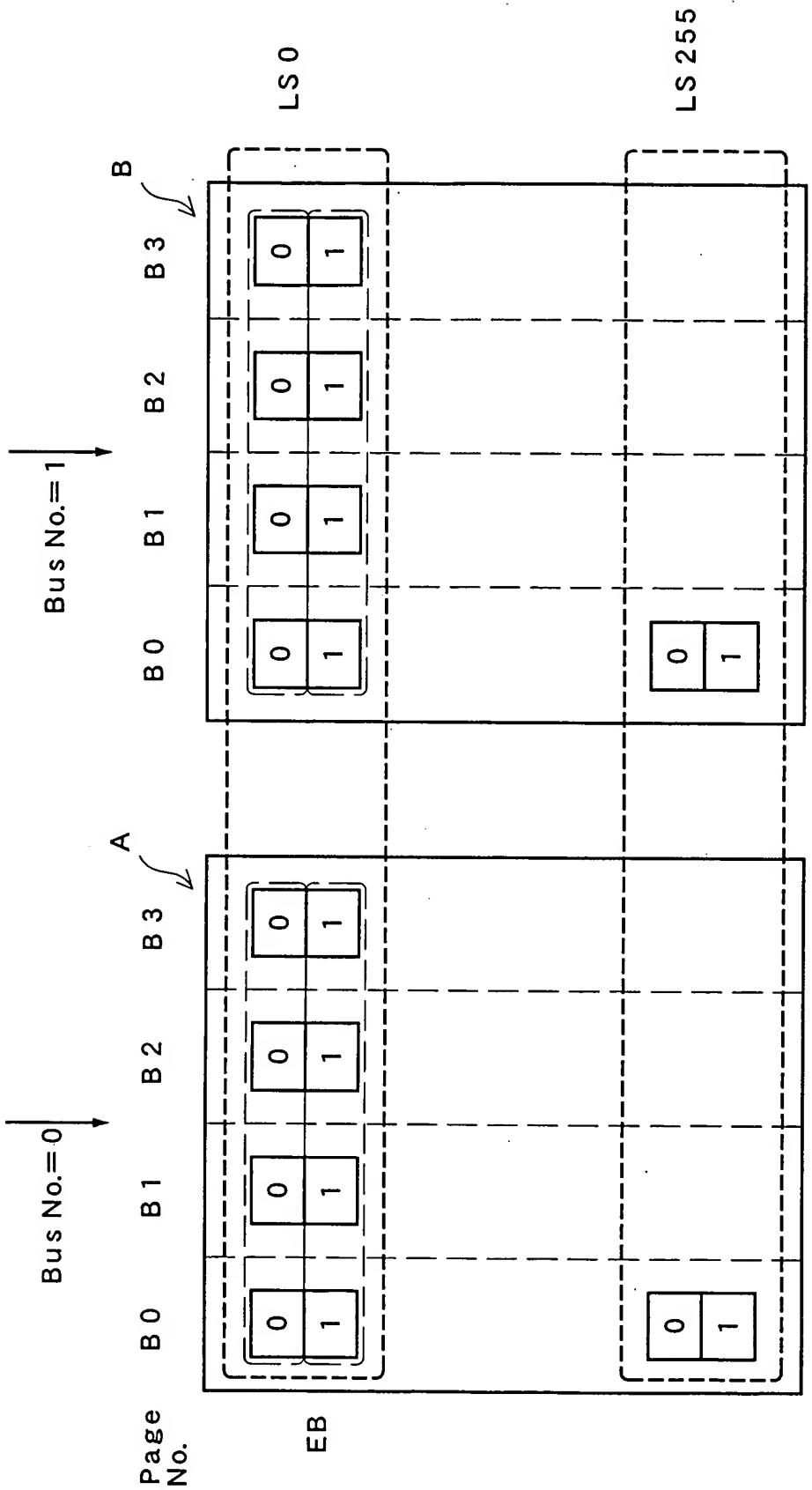

FIG. 11

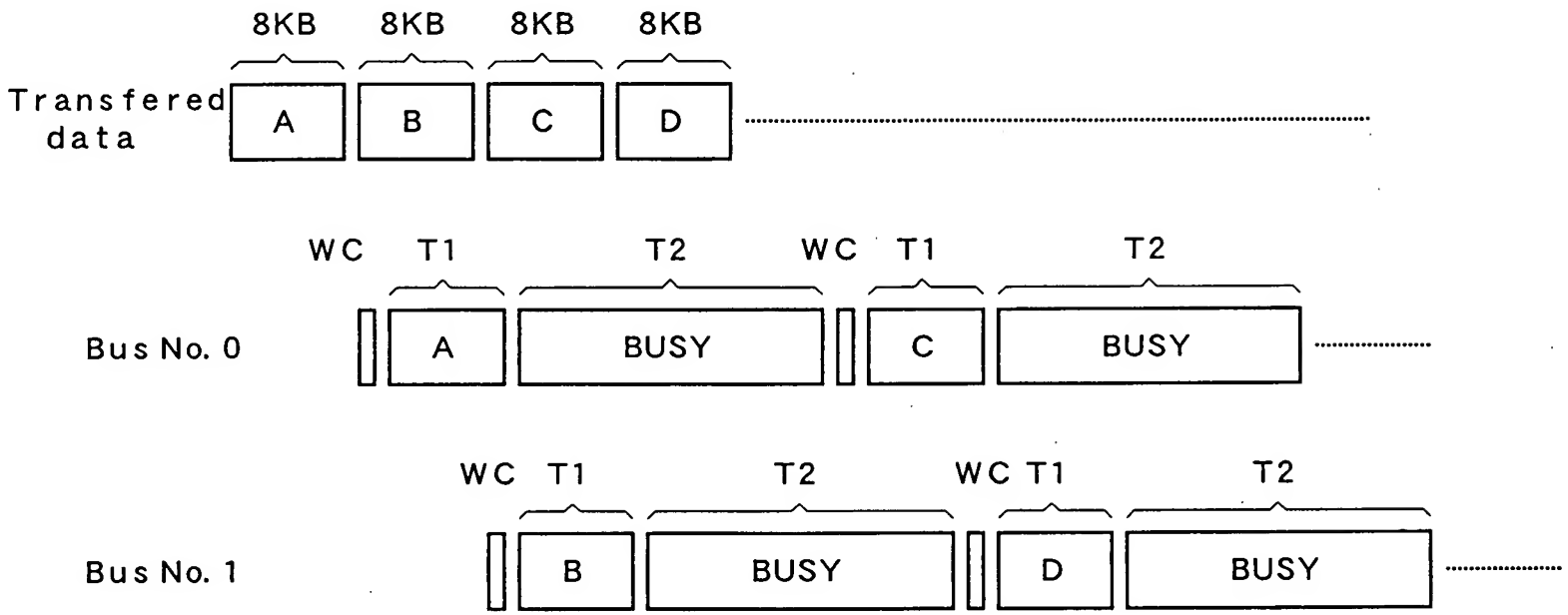

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FIG. 12

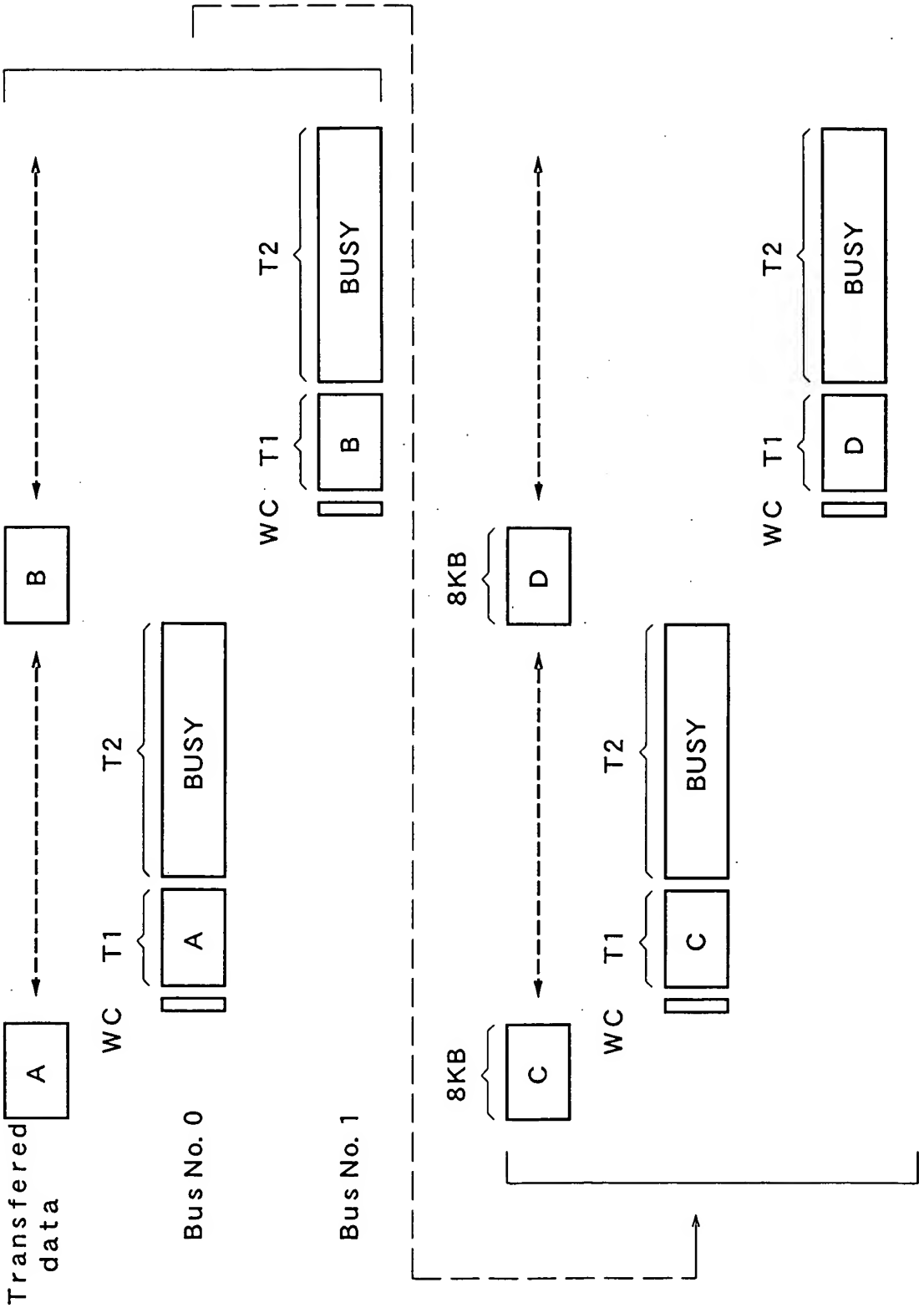

Transfered data
8KB
A
WC
T1
T2
BUSY
Bus No. 0
8KB
B
WC
T1
T2
BUSY
Bus No. 1
8KB
C
WC
T1
T2
BUSY
8KB
D
WC
T1
T2
BUSY

FIG. 13

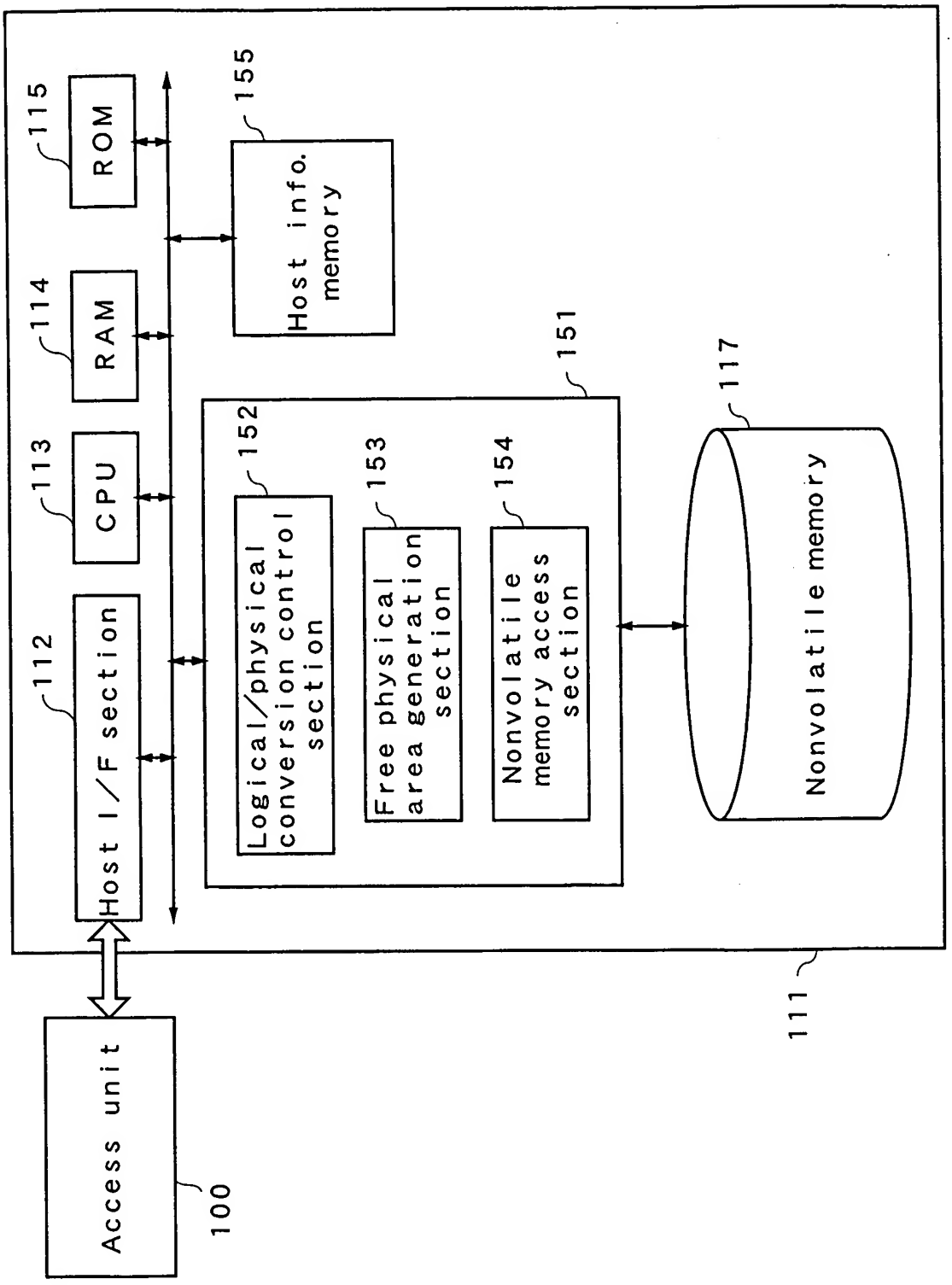

Access unit
100
Host I/F section
112
CPU
113
RAM
114
ROM
115
Logical/physical conversion control section
152
Free physical area generation section
153
Nonvolatile memory access section
154
151
Host info. memory
155
Nonvolatile memory
117
111

FIG. 14

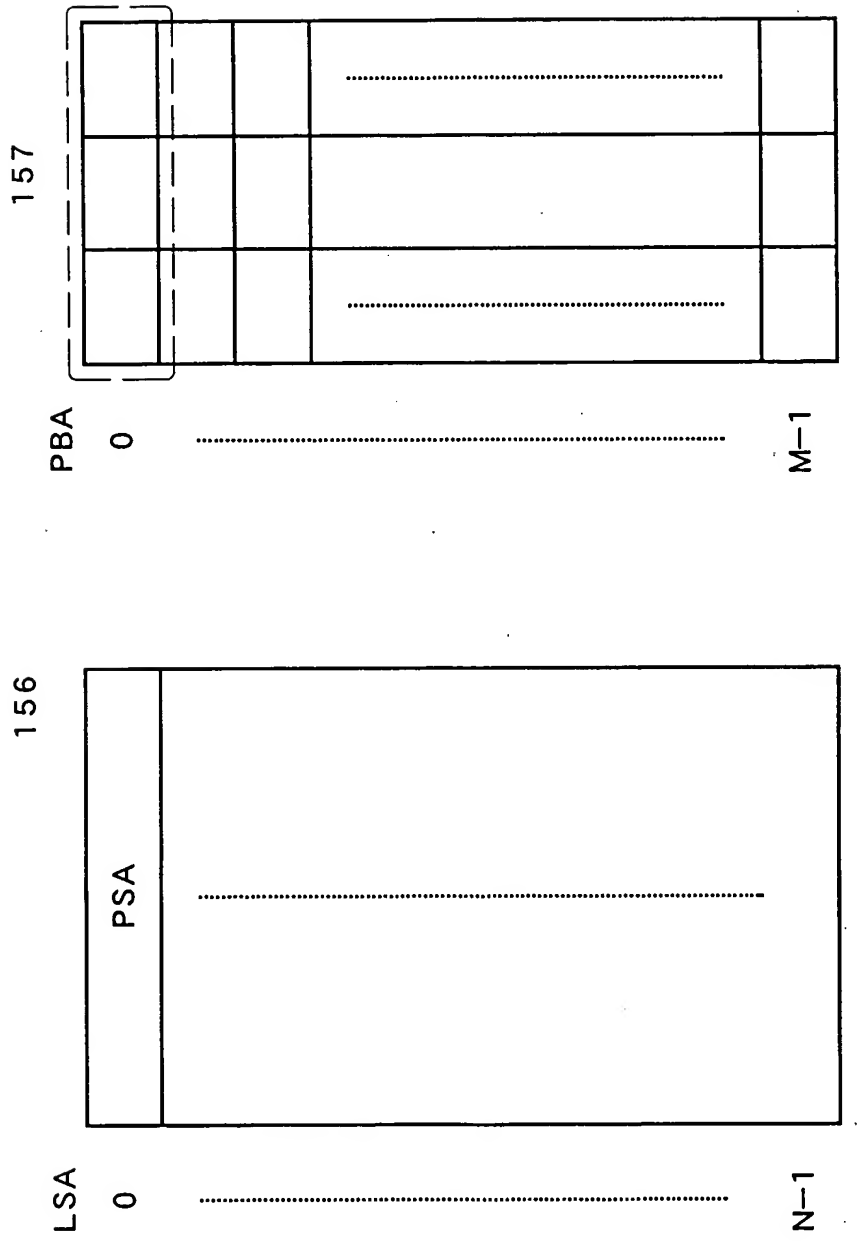


FIG. 15

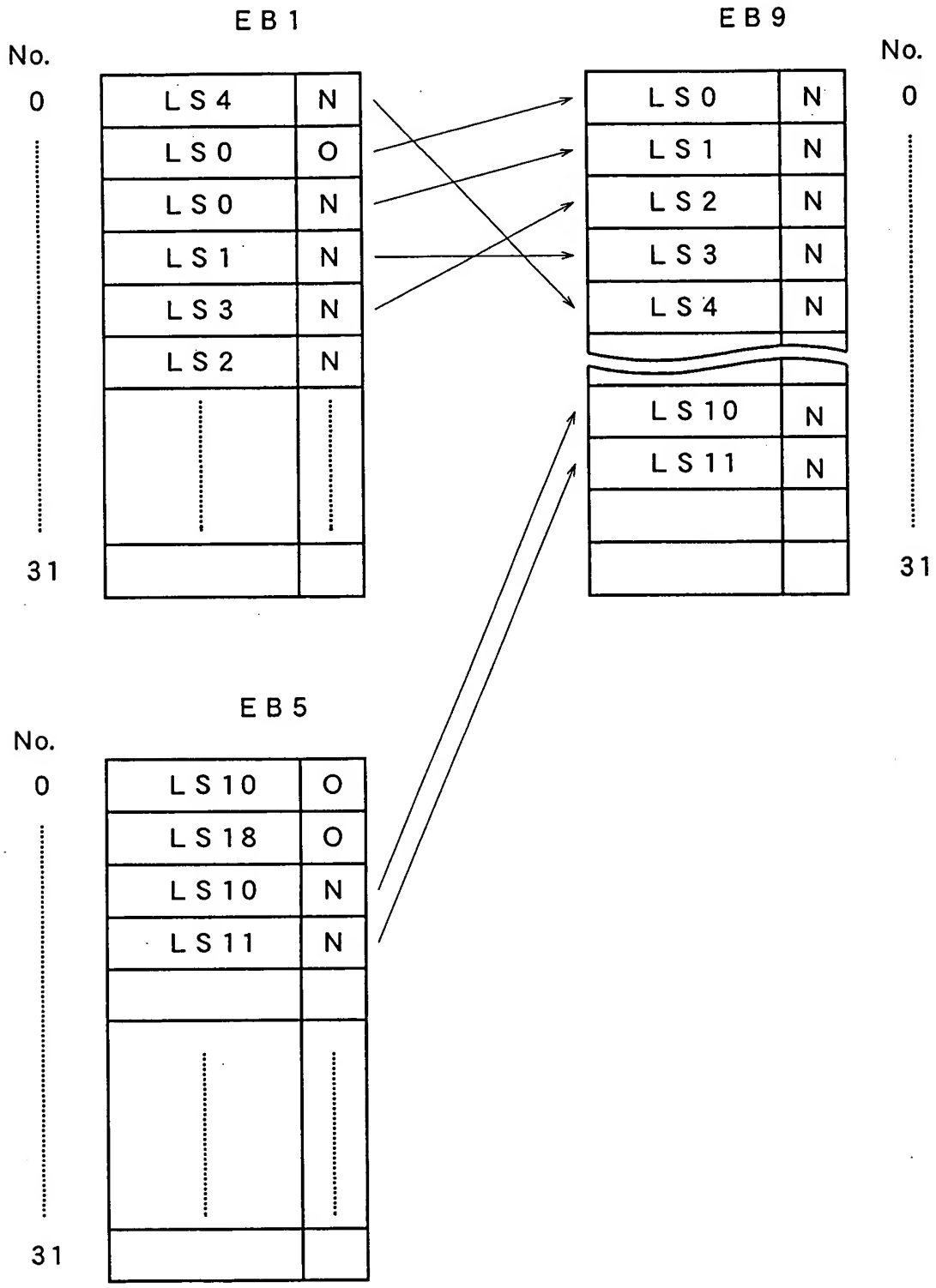

EB1
No.
0
LS4 N
LS0 O
LS0 N
LS1 N
LS3 N
LS2 N
31
EB9
No.
0
LS0 N
LS1 N
LS2 N
LS3 N
LS4 N
LS10 N
LS11 N
31
EB5
No.
0
LS10 O
LS18 O
LS10 N
LS11 N
31

FIG. 16

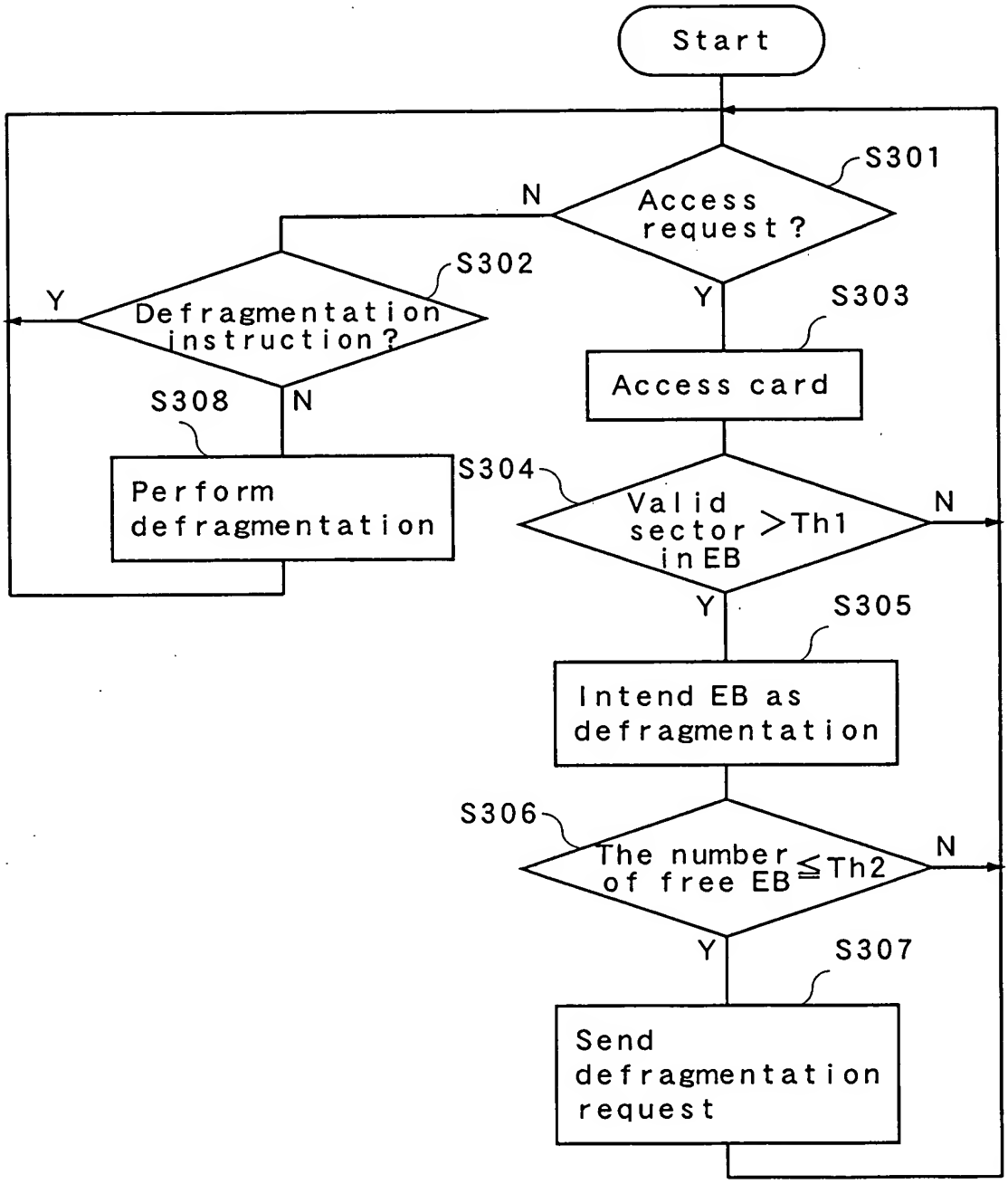

Start
S301
Access request ?
N
Y
S302
Defragmentation instruction ?
Y
N
S303
Access card
S308
Perform defragmentation
S304
Valid sector in EB > Th1
N
Y
S305
Intend EB as defragmentation
S306
The number of free EB ≦ Th2
N
Y
S307
Send defragmentation request

FIG. 17

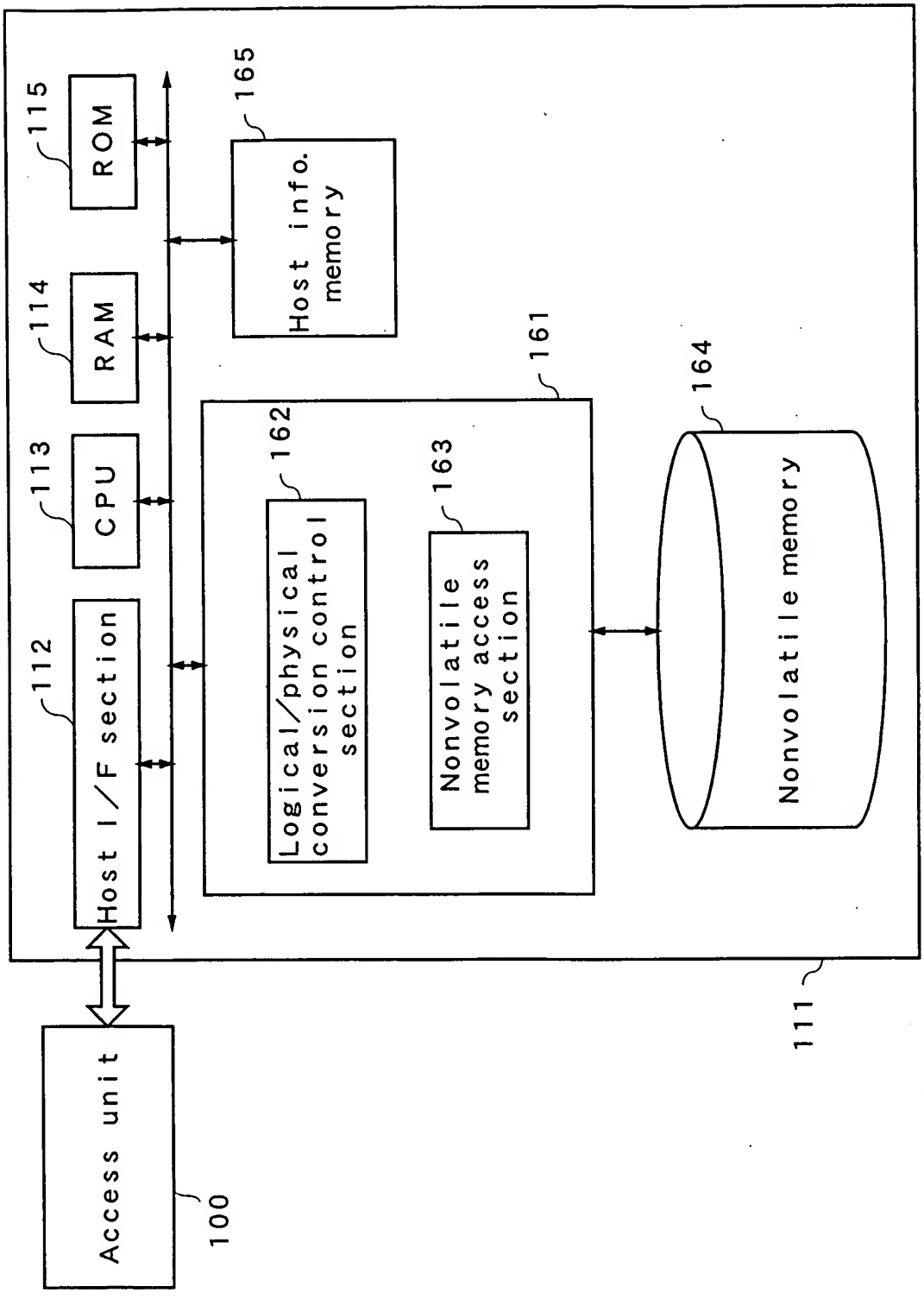

Access unit
100
Host I/F section
112
CPU
113
RAM
114
ROM
115
Host info. memory
165
161
Logical/physical conversion control section
162
Nonvolatile memory access section
163
Nonvolatile memory
164
111

FIG. 18

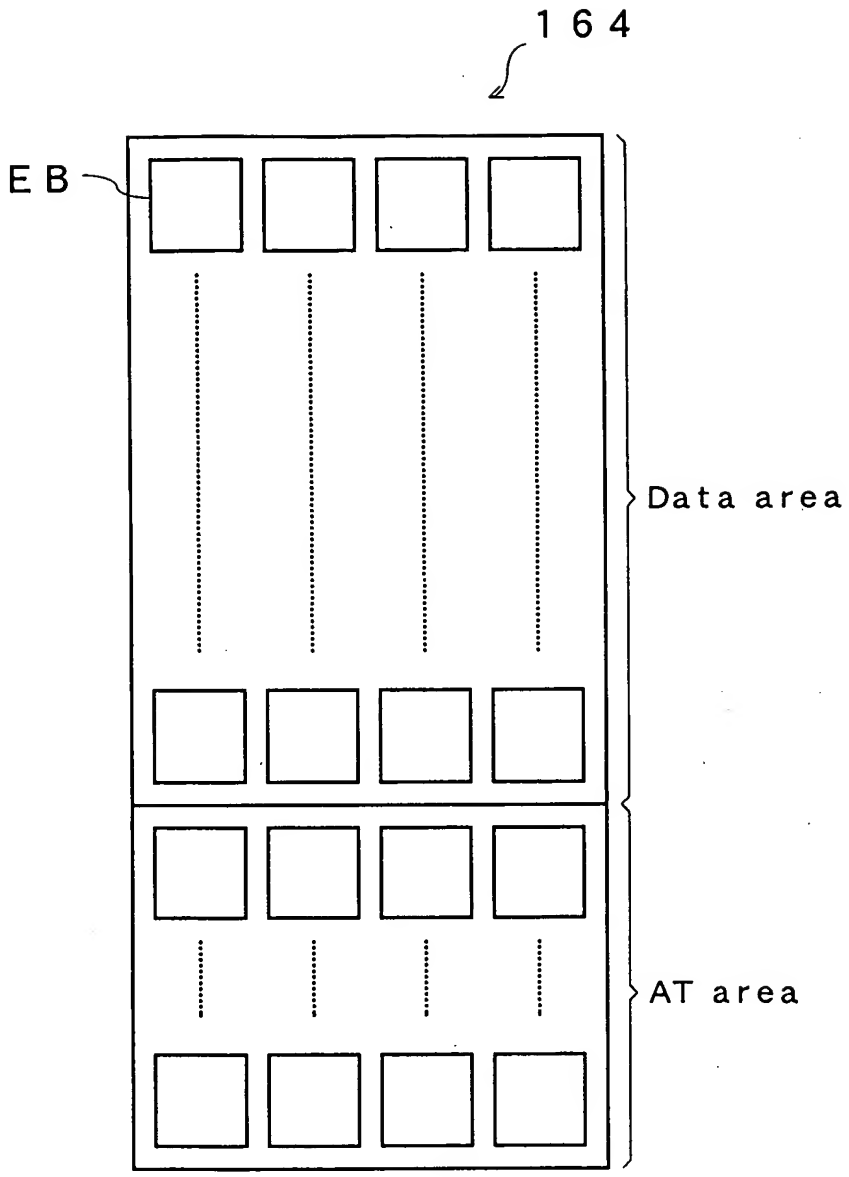


FIG. 19

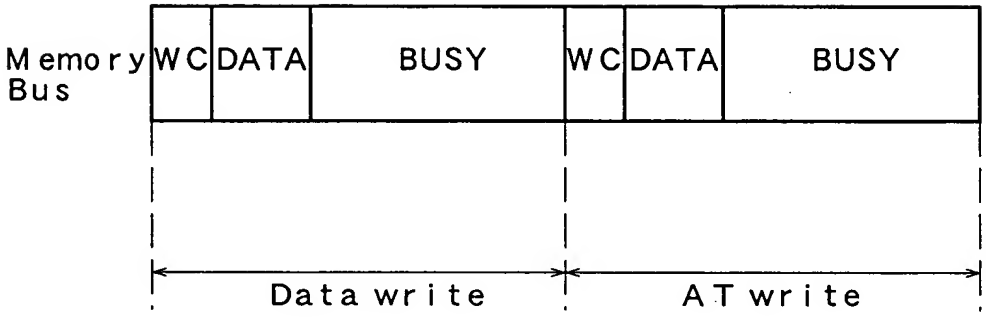
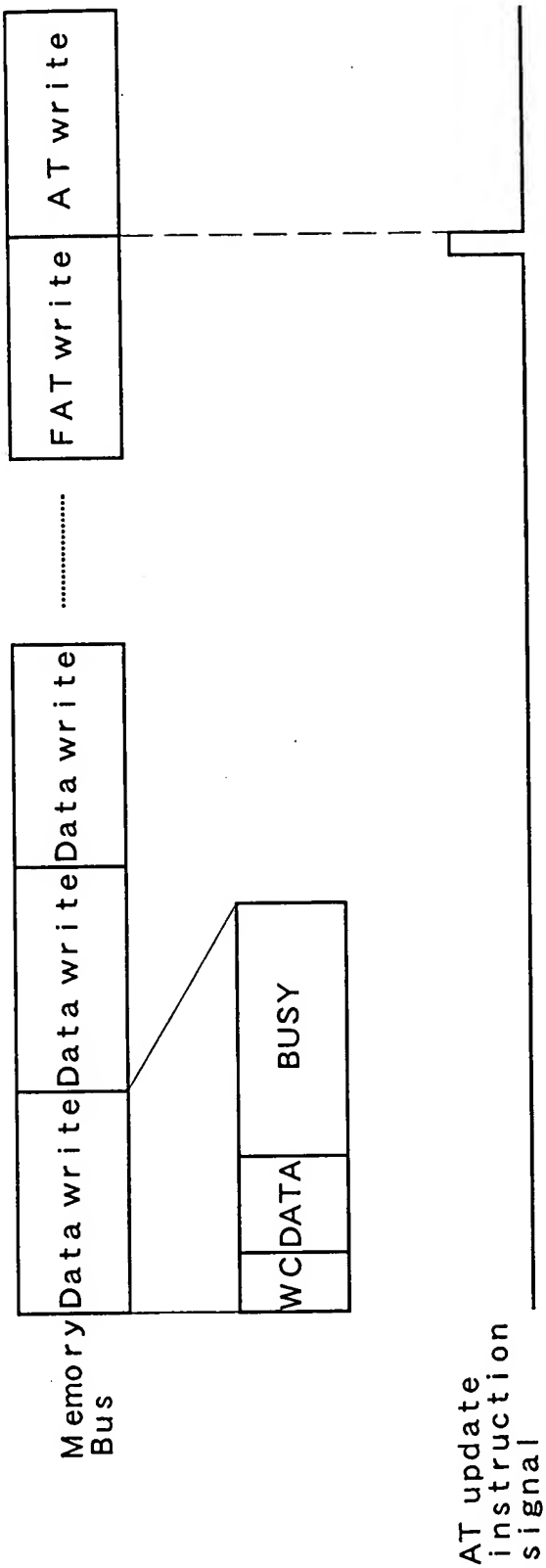


FIG. 20


Memory Bus
AT update instruction signal
Data write
Data write
Data write
Data write
WC
DATA
BUSY
FAT write
AT write